Attorney Docket No.: MICRON-01023

## DECLARATION FOR PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name. I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: ON-CHIP SUBSTRATE REGULATOR TEST MODE. The specification of which (check one)  $\underline{x}$  is attached hereto or  $\underline{x}$  was filed on as Application Serial No. and was amended on (if applicable). I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

			Priority Claim
Prior Foreign Application(s)			Yes No
Number	Country	Day/Month/Year Filed	
I hereby claim the benefit under Title subject matter of each of the claims of first paragraph of Title 35, United Sta of Federal Regulations, § 1.56(a) while date of this application:	of this application is not disclosed in ates Code, § 112, I acknowledge the	the prior United States application in duty to disclose material information	n the manner provided by the n as defined in Title 37, Code
Application Serial No.	Filing Da	te Status: P	atented, Pending, Abandoned
I hereby declare that all statements medieved to be true; and further that the punishable by fine or imprisonment of may jeopardize the validity of the appropriate the validity of the approp	hese statements were made with the lor both, under Section 1001 of Title plication or any patent issued thereor	knowledge that willful false statements of the United States Code and the	nts and the like so made are
Inventor's Signature:	H. llam		8-16-95
Inventor's Signature. 11000	1/100.001.1		Date
Residence: 6410 Randolph Drive	Boise, Idaho 83709		
Citizenship: USA  Post Office Address: 8000 S. Fed	eral Way, Boise, Idaho 83706		
LOST OTHER WORLSZ. OOOO 2: LCO	ciai way, Doise, Idano 65700		<del></del>

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Group: ) Art Unit:			
Gary Gilliam	) Examiner:			
Serial No.:	)			
Filed: Filed Herewith	) ) POWER OF ATTORNEY BY ASSIGNEE )			
For: ON-CHIP SUBSTRATE REGULATOR TEST MODE	) ) 			
Honorable Commissioner of Patents and Trademark Washington, D.C. 20231	as .			
Sir:				
00/1/05	nee of the above-identified application by Assignment dated as,(Reg. No. 34,095) and also the members of the firm of			
HAVERSTOCK & ASSOCIATES a firm including	Thomas B. Haverstock (Reg. No. 32,571) and Jonathan O.			
Owens (Reg. No. 37,902), 260 Sheridan Avenue, S	uite 420, Palo Alto, California 94306, (415) 833-0160, as its			
attorneys with full power of substitution to prosecu	te this application and to transact all business in the Patent			
and Trademark Office in connection therewith.				
Please direct all correspondence regarding this application to the following:				
Thomas B. Haverstock HAVERSTOCK & ASSOCIATES 260 Sheridan Avenue, Suite 420 Palo Alto, California 94306 Telephone: (415) 833-0160 Facsimile: (415) 833-0170	S .			
	nent filed with the application or filed subsequent to the filing reby certify that, to the best of my knowledge and belief, title			
MICRON TECHNOLOGY, INC.				

Dated: August 29, 1995

By: W. Bryan Farney

Name: W. Bryan Farney

Title: Vice President of Legal Affairs and General Counsel